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Transmitted herewith for filing is the patent application of:

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For: METHODS FOR FORMING AND INTEGRATED CIRCUIT STRUCTURES CONTAINING RUTHENIUM AND TUNGSTEN CONTAINING LAYERS

Enclosed are:

☒ 12 pages of specification, 9 pages of claims, an abstract, a Declaration of Inventor for Patent Application, and a Power of Attorney By Assignee and Certificate By Assignee Under 37 CFR § 3.73(b).
☒ 4 sheet(s) of formal drawings.
☒ An assignment of the invention to: Micron Technology, Inc. and a Recordation Cover Sheet.

		FILING FEE				
	Claims	Number		Number		Basic Fee
For	Filed	Free		Extra	Rate	$690.00
Total Claims	71	20	=	51	$18.00	$918.00
Independent Claims	24	3	=	21	$78.00	$1,638.00
Multiple Dependent Claim Fee					$260.00	$0.00
TOTAL FILING FEE						$3,246.00

☒ A check in the amount of $3,286.00 to cover ☒ filing fee and ☒ assignment recordal fee is enclosed.

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Respectfully submitted,

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METHODS FOR FORMING AND INTEGRATED CIRCUIT STRUCTURES CONTAINING RUTHENIUM AND TUNGSTEN CONTAINING LAYERS

Field

The invention pertains to semiconductor devices and the fabrication thereof, and particularly to ruthenium- and tungsten-containing electrically conductive layers and the formation and use thereof.

Background

A capacitor generally includes two electrical conductors in close proximity to, but separated from, each other. The two conductors form the "plates" of the capacitor, and may be separated by a dielectric material. When a voltage is applied across the plates of a capacitor, electrical charge accumulates on the plates. If the plates are electrically isolated essentially immediately after a voltage is applied, the accumulated charge may be stored on the plates, thus "storing" the applied voltage difference.

The fabrication of integrated circuits involves the formation of electrically conductive layers for use as various circuit components, including for use as capacitor plates. Memory circuits, such as DRAMs and the like, use electrically conductive layers to form the opposing plates of storage cell capacitors.

The drive for higher-performance, lower-cost integrated circuits dictates ever-decreasing area for individual circuit features, including storage capacitors. Since capacitance of a capacitor (the amount of charge that can be stored as a function of applied voltage) generally varies with the area of capacitor plates, as the circuit area occupied by the storage capacitor decreases, it is desirable to take steps to preserve or increase capacitance despite the smaller occupied area, so that circuit function is not compromised.

Various steps may be taken to increase or preserve capacitance without increasing the occupied area. For example, material(s) having higher dielectric constant may be used between the capacitor plates. Further, the plate surfaces may be roughened to increase the effective surface area of the plates without increasing the area occupied by he capacitor.

One method for providing a roughened surface for a plate of a storage cell capacitor is to form the plate of hemispherical grain polysilicon (HSG), possibly with an

overlying metal layer. The hemispherical grains of HSG enhance the surface area of the plate without increasing its occupied area.

HSG presents difficulties in fabrication, however, because of the formation of silicon dioxide on and near the HSG. A silicon dioxide layer may form on the HSG, particularly during deposition of the capacitor's dielectric layer. Even with an intervening metal layer present, oxygen from the deposition of the dielectric layer can diffuse through the metal layer, forming silicon dioxide at the polysilicon surface. Silicon diffusion through the metal layer may also produce a silicon dioxide layer between the metal and the dielectric layers.

Silicon dioxide between the metal layer and the HSG can degrade the electrical contact to the metal capacitor plate surface. Silicon dioxide between the metal layer and the dielectric layer can decrease the capacitance of the resulting capacitor.

To attempt to avoid these negative effects caused by formation of silicon dioxide, a diffusion barrier layer may be employed between the HSG and the metal layer. However, in the typical capacitor geometry, the greater the total number of layers, the larger the required minimum area occupied by the capacitor. Further, the upper surface of each additional layer deposited tends to be smoother than the underlying surface, reducing the increased surface area provided by an underlying rough layer.

While high-dielectric constant materials are known, many of these advantageous materials are formed with processes that are incompatible with other materials needed to form capacitors. For example, processes needed to form a particular dielectric layer can oxidize or otherwise impair the properties of the electrode layer on which the dielectric layer is to be formed. These processes can be incompatible because of the necessary process temperatures or process ambients.

For these reasons, improved materials and methods are needed for forming conducting layers, insulating layers, and capacitors using such layers.

Summary

The present invention provides improved conductive layers, dielectric layers, capacitors, methods for forming such layers, and capacitors using the layers.

In a representative embodiment, enhanced-surface-area (rough-surfaced) ruthenium containing electrically conductive layers are provided. These layers are compatible with high-dielectric-constant materials and are useful in the formation of integrated circuits, particularly for plates of storage capacitors in memory cells.

In one approach, the enhanced-surface-area electrically conductive layer may be formed by first forming a ruthenium oxide containing film or layer. The layer may be stoichiometric or non-stoichiometric, and may be amorphous or may have both ruthenium (Ru) and ruthenium oxide (RuO_2) phases and may include other materials. The film may be formed, for example, by chemical vapor deposition techniques or by sputtering or any suitable techniques. The film may be formed over an underlying layer which may be electrically conductive.

The ruthenium oxide film may be processed at low pressure and high temperature—generally at pressures at least about 75 torr or below, desirably about 20 torr or below, most desirably about 5 torr or below—and at temperatures in the range of about 500 to 900°C, desirably about 750 to about 850°C—so as to convert at least some of the ruthenium oxide to ruthenium and to yield a roughened ruthenium-containing layer with a mean grain size desirably in the range of about 100 Angstroms or larger.

The heating process, or anneal, is desirably performed in a non-oxidizing ambient. In an example embodiment, a nitrogen-supplying ambient or nitrogen-supplying reducing ambient may be used during the anneal. A nitrogen-supplying reducing ambient may be used to passivate the ruthenium for improved compatibility with high-dielectric-constant dielectric materials. In another alternative, a nitrogen-supplying reducing ambient may be used in a post-anneal to passivate an already roughened layer. In still another alternative, a post-anneal in an oxidizing ambient may be performed, following either the roughening anneal or the nitride-passivation anneal, as desired. This oxidizing post-anneal provides oxygen to the roughened layer to reduce the tendency of the ruthenium to scavenge oxygen during later processing.

The enhanced-surface-area layer may be formed with or without a pre-anneal, performed at a higher pressure (such as about 600 torr), before the low pressure, high temperature anneal.

The roughened layer of ruthenium may be used to provide an enhanced-surface-area electrically conductive layer.

In an example embodiment, the roughened layer of ruthenium may be formed on an underlying electrically conductive layer, with the roughened layer and the underlying layer together functioning as an enhanced-surface-area electrically conductive layer.

In another example embodiment, an electrically conductive layer may be formed on or over the roughened layer, with the overlying electrically conductive layer and the roughened layer constituting an enhanced-surface area electrically conductive layer.

In either case, in an example capacitor embodiment for use in an integrated circuit, the resulting enhanced-surface-area electrically conductive layer may be used to form a plate of a storage capacitor in an integrated circuit, such as in a memory cell of a DRAM or the like.

The ruthenium-containing enhanced-surface-area electrically conductive layer, particularly in the case of an anneal in nitrogen-supplying reducing ambient with an oxidizing post-anneal, has reduced tendency toward oxidation and is thus more compatible with the use of high-dielectric-constant dielectric materials, while still providing enhanced surface area. In addition, even if the ruthenium-containing layer oxidizes, it remains conductive. An additional metal layer thus may potentially be omitted from the capacitor structure, allowing smaller dimensions for capacitors with the same or even greater capacitance.

In an alternative embodiment, a tungsten nitride layer is provided as a first electrode layer. A dielectric layer and a second electrode layer are conformally applied to the first electrode layer to form a capacitor. The capacitor, or at least the tungsten nitride layer, is annealed at an anneal temperature to increase the capacitance of the capacitor. In a specific embodiment, the anneal temperature is at least 500 C and the capacitor (or the tungsten nitride layer) is maintained at the anneal temperature for at least 30 seconds.

These methods, conductive and dielectric layers, and structures using the layers allow the design and fabrication of higher speed, higher density, and lower cost integrated circuits.

Brief Description of the Drawings

FIG. 1 is a partial cross-section of layers used in a process according to one embodiment, the layers including a ruthenium oxide containing layer.

FIG. 2 is a cross-section of the layers of FIG. 1 after a low-pressure, high-temperature anneal, including a roughened layer.

FIG. 3 is a partial plan view of the layers of FIG. 2

FIG. 4 is a cross-section similar to that of FIG. 2 but having an additional layer underlying the roughened layer.

FIG. 5 is a cross section of the layers of FIG. 2 after formation of an additional layer overlying the roughened layer.

FIG. 6 is a cross section of an enhanced-surface-area electrically conductive layer with a dielectric layer formed thereon according to one embodiment.

FIG. 7 is a cross section of the layers of FIG. 6 with an electrically conductive layer formed on the dielectric layer.

FIGS. 8A-8B are cross-sections of two embodiments of capacitor structures that include a roughened layer.

FIGS. 9A-9C are cross-sections of capacitor structures that include a tungsten nitride electrode layer.

Detailed Description

The present invention allows creation of a surface-area-enhanced ruthenium electrically conductive layer that has improved compatibility with high-dielectric-constant ("high-κ") dielectric materials as compared to hemispherical-grain polysilicon (HSG).

The surface-area-enhanced electrically conductive layer is created by heating a film or layer comprising ruthenium oxide such as the layer 12 of FIG. 1. The heating process, which may anneal the film or layer, is typically performed at low pressures of less than about 75 torr, desirably less than about 20 torr, and most desirably less than about 5 torr, and at high temperatures in the range of about 500 to 900°C, desirably about 750 to 850°C. The treatment is desirably performed in a non-oxidizing ambient. The heating process may be performed in a noble ambient, nitrogen ambient, or the like, or in a reducing ambient, which may reduce the temperature required. The heating process may also be performed in an electrically neutral environment, or with plasma or glow-discharge assistance or the like, which may also reduce the temperature required. Heating under relatively low pressure converts at least a portion of the ruthenium oxide to ruthenium and produces a rough surface on the layer. Temperature and pressure are preferably selected so as to enhance the ruthenium oxide to ruthenium conversion.

The surface-area-enhanced electrically conductive layer may be formed on a supporting structure 10 shown in partial cross-section in FIG. 1. The supporting structure 10 may be any structure present in or on an integrated circuit during the fabrication thereof. In a typical example application, the supporting structure may be an electrically conductive material that will be in electrical contact with a capacitor plate formed by the surface-area-enhanced electrically conductive layer.

The ruthenium oxide layer 12 may be formed by any suitable method. Specific examples of such methods include chemical vapor deposition (CVD) or related process, or sputtering or related process, or the like. The ruthenium oxide layer may be stoichiometric ruthenium oxide (RuO_2) or non-stoichiometric ruthenium oxide (RuO_x).

If the layer 12 is formed via CVD, the deposition may be performed, for example, at pressures of 1-20 torr, desirably about 5 torr. The oxygen may be supplied in the form of O_2 or other oxidizing gas, such as N_2O, NO, or ozone (O_3). The oxygenating gas and a ruthenium precursor, and suitable diluent gasses, if desired, may be supplied at suitable flow rates, such as in the range of about 100-2000 sccm. Alternatively, the ruthenium precursor can be deliver by direct vaporization. Deposition may be performed for a time in the range of about 10 to 500 seconds, desirably for sufficient time and under sufficient conditions to deposit RuO_x or RuO_2 to a thickness in the range of about 100 to 600 Angstroms.

The resulting ruthenium oxide layer 12 may optionally be pre-annealed, such as by rapid thermal anneal (RTA) in hydrogen or other suitable anneal environment at pressures in the range of 500 to 700 torr and temperatures in the range of 500 to 900°C. The pre-anneal stabilizes the film, promoting crystallization of ruthenium and ruthenium oxide phases.

The ruthenium oxide layer 12, with or without a pre-anneal, is then treated at low pressure and high temperature as described above. The treatment may reduce the proportion of ruthenium oxide in the layer and increase the proportion of ruthenium. The ruthenium oxide in the ruthenium oxide layer 12 is partially or completely converted to ruthenium by the anneal, leaving an enhanced-surface-area layer 16 shown in the cross section of FIG. 2. While the enhanced-surface-area layer 16 is referred to by separate reference character for convenience herein, it should be noted that the layer 16 is formed from the layer 12, and is the same layer in that sense. FIG. 3 shows a partial plan view of the roughened ruthenium layer 16 of FIG. 2. Although the example roughened ruthenium layer 16 shown in the figures is discontinuous, this is by way of example only and continuous films may also be produced. Increased thickness of the initial layer 12 tends to produce more continuous films, as does reduced temperature and increased pressure during the anneal and reduced anneal time.

The anneal may be performed in a noble, nitrogen, or reducing ambient or the like. As an additional example embodiment, an anneal may be performed in a nitrogen-supplying reducing ambient such as such as ammonia, nitrogen, a nitrogen and hydrogen mixture, and the like. The anneal parameters may be selected such that "nitrogen-passivated" ruthenium in the form of RuN_x is formed in the layer 16, at least near the outermost surfaces thereof, passivating the layer 16.

As another example alternative, nitride passivation may be used in the form of a post-anneal in a nitrogen-supplying reducing ambient.

As yet another variation, a desirably brief post-anneal in an oxidizing ambient such as oxygen or ozone may be performed on the already roughened layer 16, to form "oxygen-passivated" ruthenium or ruthenium nitride in the outermost portions of the layer 16 (RuO_xN_y or RuO_x), in order to reduce or prevent the ruthenium from later scavenging oxygen from a nearby dielectric material. The oxidizing post-anneal may optionally follow a nitride passivation post-anneal.

As indicated in FIG. 2, the roughened ruthenium layer 16, together with the supporting structure 10 if electrically conductive, may together constitute an enhanced-surface-area electrically conductive layer 26 compatible with high-dielectric-constant dielectric materials.

The layer 16 produced such as described above may also be used in cooperation with other layers. This may be useful in cases where the supporting structure 10 may not be electrically conductive or may be incompatible with high-dielectric-constant dielectric materials. In the discussion and claims herein, "on" used with respect to two layers, one "on" the other, means at least some contact between the layers, while "over" means the layers are in close proximity, but possibly with one or more additional intervening layers such that contact is not required. Neither "on" nor "over" implies any directionality as used herein.

As shown, for example, in FIG. 4, a layer 22 of material may be formed over the supporting structure 10, with the roughened ruthenium layer 16 then formed on the layer 22. The layer 22 may be an electrically conductive layer to electrically connect all portions of layer 16. The layer 22 may also act as a barrier layer to prevent contact between high-dielectric-constant dielectrics, to be used for capacitor formation, and the supporting structure 10. If the layer 22 is an electrically conductive layer, layer 22 together with layer 16 constitute an enhanced-surface-area electrically conductive layer 26. Any compatible electrically conductive material may be used, such as Pt, Ir, IrO_x, Rh, $RuSi_x$, and $SrRuO_x$ and alloys thereof as well as $RuSiO_x$ and $RuSiN_x$, for example.

Alternatively, as shown for example in FIG. 5, a layer 24 of electrically conductive material may be formed conformally over the layer 16 and over the supporting structure 10. The layer 24, together with the layer 16, then constitutes an enhanced-surface-area electrically conductive layer 26. As with the layer 22, the layer 24 may function to electrically connect all portions of layer 16, and may also function as a barrier

layer to prevent contact between high-dielectric-constant dielectrics and the supporting structure 10. Examples of such electrically conductive materials include the materials listed in the preceding paragraph. Ruthenium oxide is a desirable material because of compatibility with the underlying ruthenium layer 16.

As described by way of example above with reference to FIGS. 3-6, the supporting structure 10 and/or one or more layers above or below the layer 16 (or both) may be electrically conductive and may be employed as needed to obtain conductivity and other desired properties. The resulting enhanced-surface-area electrically conductive layer 26, shown by way of example in FIGS. 3, 5, and 6, is represented generically as layer 26 in FIG. 6. To form a capacitor with the enhanced-surface-area electrically conductive layer 26, a layer 28 of dielectric material, most desirably a high-dielectric-constant dielectric material (generally any dielectric with a dielectric constant of at least 9), such as tantalum pentoxide (Ta_2O_5), may be formed conformally over the enhanced-surface-area electrically conductive layer, as shown in FIG. 6. Other high-constant dielectrics may also be employed, such as barium strontium titanium oxide $(Ba,Sr)TiO_3$, lead zirconium titanium oxide $Pb(Zr,Ti)O_3$, and strontium bismuth tantalum oxide ($SrBi_2Ta_2O_9$), for example. The layer 28 is desirably sufficiently thin and conforming to provide an at least somewhat enhanced surface area on the surface away from the layer 26.

An electrically conductive layer 30 may then be formed conformally over the dielectric layer 28, as shown in FIG. 7. The surface of layer 30 uppermost in the figure is not shown because the layer may generally be of any thickness sufficiently thick to insure continuity of the layer and sufficiently thin to fit within the overall volume allotted to the capacitor. As shown in FIG. 7, the surface of layer 30 next to the dielectric layer 28 desirably conforms to the enhanced surface area of the dielectric layer 28, providing an enhanced surface area for the electrically conductive layer 30 as well. The two electrically conductive layers, layers 26 and 30, form the two plates of a capacitor. Both plates desirably have enhanced surface area relative to the area occupied by the capacitor.

Application of the plate structure shown in FIG. 7 to a container capacitor is illustrated in the cross-section of a container capacitor shown in FIG. 8A. The supporting structure 10 may be an electrically conductive plug of polysilicon or other electrically conductive material formed at the bottom of an opening in a dielectric material 32 such as borophosphosilicate glass (BPSG). The lower end of the plug typically electrically contacts a circuit element such as a transistor gate (not shown). At the sides of the

cylindrical container, the BPSG itself functions a supporting structure for the capacitor plate structure. The relative thinness of the capacitor structure provided by the layer structure of FIG. 7 maximizes the capacitor plate surface area in the container capacitor of FIG. 8A, particularly for the inner (upper) electrode, the surface area of which decreases most rapidly with increasing thickness of the layer structure. The use of the enhanced-surface-area ruthenium electrically conductive layer thus provides improved capacitance in a given area.

Application of the plate structure shown in FIG. 7 to a stud capacitor is illustrated in the cross-section of a stud capacitor shown in FIG. 8B. The supporting structure 10 includes a plug 25 that extends from a surface 27 and the layers 26, 28, 30 are formed conformally on the plug 25.

In a specific example, ruthenium oxide was deposited on substrates of BPSG to a thickness of about 600 Angstroms by CVD. The ruthenium oxide layers were pre-annealed in nitrogen for one minute at 800°C and 600 torr, then annealed at 800°C in nitrogen for varying times and at varying pressures. Such a pre-anneal can be omitted.

On SEM examination, layers annealed for eight minutes at 4.5 torr showed marked surface roughness with mean grain size of about 100 Angstroms or larger, with good uniformity over the substrate surface. Layers annealed for eight minutes at 60 torr showed some surface roughness with a mean grain approaching 100 Angstroms, but with generally less roughness than at 4.5 torr. Layers annealed for eight minutes at 600 torr showed generally still less roughness and still smaller grain sizes than at 60 torr. Layers annealed for two minutes at 4.5 torr also showed a marked surface roughness, with possibly slightly less uniformity over the substrate surface than those annealed for eight minutes. X-ray diffraction studies of the annealed layers showed ruthenium as the primary constituent but the Ru/RuO_2 ratio varied with processing conditions.

Superior capacitors including metal-insulator-metal (MIM) capacitors can be obtained using a tungsten nitride layer as an electrode. The tungsten nitride layer can be formed by reactive sputtering of a tungsten target in a nitrogen containing ambient, or by a chemical vapor deposition process (CVD) such as a plasma enhanced CVD (PECVD), a metallo-organic CVD (MOCVD) process, atomic layer deposition (ALD), or other process. The tungsten nitride layer is conveniently formed using a thermal CVD process using tungsten fluoride (WF_6) and ammonia (NH_3) as precursors, and a 300 Angstrom thick layer can be formed using such a process in about 1-3 minutes. The thickness of the

tungsten nitride layer can be varied but typically the thickness is in the range of 100-1000 Angstroms.

As deposited, the tungsten nitride layer can contain a mixture of a stable tungsten nitride compound W_2N and a metastable tungsten nitride compound WN. The metastable compound WN can be converted to the stable tungsten nitride compound W_2N in a rapid thermal process (RTP) in which the temperature of the tungsten nitride layer is rapidly raised to an anneal temperature in the range of 600-800 C and held at the anneal temperature for about 60 seconds. Typically, the temperature of the tungsten nitride layer is ramped up to and down from an anneal temperature of 700 C in less than about 30 seconds. Such an anneal process is typically performed before a dielectric layer and a second electrode are formed on the tungsten nitride layer so that a capacitor structure is otherwise complete. The metastable compound WN may include defects and may be preferentially oxidized during deposition of dielectric materials such as Ta_2O_5 and subsequent annealing processes. Therefore, the capacitance of a capacitor formed without an anneal process tends to be low. In addition, the presence of defects tends to increase leakage currents. In a completed capacitor, the anneal process tends to increase capacitance by about 20% with respect to a capacitor without annealing and to reduce leakage currents that occur when voltages are applied to the electrodes.

A dielectric layer consisting of any of various dielectric materials is formed on the tungsten nitride layer. Suitable dielectric materials include high-dielectric-constant materials such as tantalum pentoxide (Ta_2O_5), doped Ta_2O_5 such as Ti-doped Ta_2O_5, barium strontium titanium oxide (Ba,Sr)TiO_3, lead zirconium titanium oxide Pb(Zr,Ti)O_3, strontium bismuth tantalum oxide ($SrBi_2Ta_2O_9$), $BaTiO_3$, $SrTiO_3$, Pb(Zr,Ti)O_3, $SrBi_2Ta_2O_9$, $SrBi_2Nb_2O_9$, $SrBi_2(Nb,Ta)_2O_9$, (Pb,La)(Zr,Ti)O_3, Al_2O_3, ZrO_2, HfO_2, and SiO_xN_y. For Ta_2O_5, formation of a stoichiometric compound is preferred so that the Ta_2O_5 layer is not a tantalum rich layer, because tantalum rich Ta_2O_5 layers tend to be conducting, not insulating. Tantalum pentoxide dielectric layers are preferred in some applications because of its large dielectric constant and its stability. However, tantalum pentoxide is typically formed using a MOCVD process in an oxidizing ambient such as an oxygen, ozone, or N_2O ambient. While many electrode layer materials cannot be exposed to oxidizing ambients, tungsten nitride is relatively unaffected by such ambients and therefore facilitates the use of tantalum pentoxide dielectric layers.

An electrode layer of tungsten nitride or other conducting material is formed on the dielectric layer and serves as a top electrode for the capacitor. Other suitable

conducting materials include TiN, TiON, WN_x, TaN, Ta, Pt, Rh, Pt-Rh, Pt-RhO_x, Ru, RuO_x, Ir, IrO_x, Pt-Ru, Pt-RuO_x, Pt-Ir, Pt-IrO_x, $SrRuO_3$, Au, Pd, Al, Mo, Ag, polysilicon, and alloys thereof. These electrode materials can be formed by various processes. For example, ruthenium and platinum/rhodium are conveniently formed using a CVD process. After the dielectric layer and the electrode layers are formed, the capacitor is annealed as described above.

FIGS. 9A-9C illustrate several example capacitor geometries that include tungsten nitride electrodes. Referring to FIG. 9A, a plate capacitor 51 is formed on a surface of a substrate 53. The substrate 53 can be any of various substrate materials including GaAs, silicon, or BPSG. The capacitor 51 includes a first electrode 55, a second electrode 57, and a dielectric layer 59. In a representative example, the first electrode 55 is a tungsten nitride layer, the dielectric layer 58 is a Ta_2O_5 layer, the second electrode is a TiN layer, and the substrate 53 is BPSG.

When voltages are applied to electrodes of a capacitor such as the capacitor 51, some electrical current flows between the electrodes. This current is generally undesirable and is referred to as a "leakage" current. Plate capacitors having electrodes of tungsten nitride have leakage currents of as little as about 20 nA/cm^2, or as low as about 5 nA/cm^2 for capacitors having dielectric layers 100 Angstroms thick and with an applied voltage of 1 V.

With reference to FIG. 9B, a container capacitor 61 is formed in an etched recess 62 in a substrate 63. A tungsten nitride electrode layer 65 covers a bottom surface 66 and a side surface 67 of the recess 62. A Ta_2O_5 dielectric layer 69 covers the electrode layer 65, substantially filling the recess 62 and a tungsten nitride electrode layer 71 (or other conductive layer) covers the dielectric layer 69. The dimensions of the recess 62 are selected to provide a desired capacitance, and can be selected in conjunction with a minimum feature size for other circuit elements that are formed on the substrate 63. In a representative example, the recess 62 has a diameter D of 200 nm and a depth Z of 1000 nm. For these dimensions, the tungsten nitride layer is preferably about 300 Angstroms (30 nm) thick. Tungsten nitride layers thinner than about 100 Angstroms (10 nm) tend to have voids. Because of these voids, such layers do not act as continuous electrodes, reducing the capacitance of the capacitor 61. Tungsten nitride layers thicker than about 1000 Angstroms (100 nm) tend to occupy too much of the volume of the recess 62, also limiting the capacitance of the capacitor 61. For container capacitors

formed in larger recesses, thicker tungsten nitride layers can be used without sacrificing too much capacitance.

The recess 62 is generally formed in the substrate 63 with an etching process. If the substrate 63 is BPSG, the recess 62 can be formed with a dry etch process such as plasma etching. While other etching processes are possible, because the recess 62 is deeper than wide, a selected etch process is preferably anisotropic.

Referring to FIG. 9C, a stud capacitor 71 is formed on a plug 73 that extends from a surface 75 of a substrate 77. A tungsten nitride electrode layer 79 is formed on the plug 73 and is covered with a dielectric layer 81 and an electrode layer 83. The dielectric layer 81 and the electrode layer can be formed of any of the materials mentioned above. Representative materials are Ta_2O_5 and TiN for the dielectric layer 81 and the electrode layer 83, respectively. The plug 73 may be an electrically conductive plug of polysilicon or other electrically conductive material formed in a recess in the substrate 77 such as a borophosphosilicate glass (BPSG). The lower end of the plug typically electrically contacts a circuit element such as a transistor gate (not shown).

In the above examples, a tungsten nitride layer is deposited directly on a substrate such as BPSG. Alternatively, a tungsten nitride layer can be formed or deposited on a titanium nitride (TiN) adhesion layer, or other adhesion layer, to improve the bonding of the tungsten nitride layer to the substrate.

Variations within the scope and spirit of the disclosure above will be apparent to those of ordinary skill in the art. For example, the enhanced-surface-area layers can be used in ferroelectric memories to improve storage capacity. The scope of coverage is accordingly defined not by the particular example embodiments and variations explicitly described above, but by the claims below.

We claim:

1. A method of forming an enhanced-surface-area electrically conductive structure, the method comprising:

providing a layer containing ruthenium oxide;

converting at least a portion of the ruthenium oxide in the layer to ruthenium so as to produce a ruthenium-containing layer having a rough surface.

2. The method of claim 1 wherein the act of converting comprises heating the layer.

3. The method of claim 1 wherein the act of converting comprises exposing the layer to a reducing ambient.

4. The method of claim 1 wherein the act of converting comprises exposing the layer to a reduced-pressure environment.

5. The method of claim 1 wherein the step of converting comprises converting at least a portion of the ruthenium oxide in the layer to ruthenium so as to produce a layer having a textured surface with a mean feature size of at least about 100 Angstroms.

6. A method of forming an enhanced-surface-area electrically conductive structure, the method comprising:

providing a layer containing ruthenium oxide;

converting at least a portion of the ruthenium oxide to ruthenium by heating the layer in a reduced-pressure environment with a pressure of about 75 torr or less so as to produce a layer having a rough surface.

7. The method of claim 6 wherein the step of converting is performed in a reduced-pressure environment with a pressure of about 20 torr or less.

8. The method of claim 6 wherein the step of converting is performed in a reduced-pressure environment with a pressure of about 5 torr or less.

9. A method of forming an enhanced-surface-area electrically conductive structure, the method comprising:

providing a layer containing ruthenium oxide;

converting at least a portion of the ruthenium oxide to ruthenium by heating the layer to at least about 500°C in a reduced-pressure environment with a pressure of about 75 torr or less for a sufficient time so as to produce a layer having a rough surface.

10. The method of claim 9 wherein the act of converting is performed by heating the layer to at least about 750°C.

11. The method of claim 9 wherein the act of converting is performed by heating the layer to at least about 800°C.

12. The method of claim 9 wherein the act of converting is performed by heating the layer to at least about 500°C for at least about 2 minutes.

13. The method of claim 9 wherein the act of converting is performed by heating the layer to at least about 500°C for a time in the range of about 2 to about 20 minutes.

14. A method of forming an enhanced-surface-area electrically conductive structure, the method comprising:

providing a layer containing ruthenium oxide; and

converting the ruthenium oxide in the layer to ruthenium so as to produce a ruthenium-containing layer having a rough surface.

15. A method of forming an enhanced-surface-area electrically conductive structure, the method comprising:

providing a layer containing ruthenium oxide;

converting some ruthenium oxide in the layer to ruthenium so as to produce a ruthenium-containing layer having a rough surface; and

exposing the layer having a rough surface to a ambient suitable to decrease the tendency of the layer to react with surrounding material.

16. The method of claim 15 wherein the act of exposing comprises exposing the layer having a rough surface to an oxidizing ambient.

17. The method of claim 15 wherein the act of exposing comprises exposing the layer having a rough surface to nitrogen ambient.

18. The method of claim 15 wherein the act of exposing comprises exposing the layer having a rough surface to a nitrogen-supplying reducing ambient.

19. The method of claim 15 wherein the act of exposing comprises exposing the layer having a rough surface first to a nitrogen-supplying reducing ambient then to an oxidizing ambient.

20. A method of forming an enhanced-surface-area electrically conductive structure, the method comprising:

providing a layer containing ruthenium oxide; and

converting some ruthenium oxide in the layer to ruthenium by heating the layer in a reduced-pressure environment in a non-oxidizing ambient so as to produce a ruthenium-containing layer having a rough surface.

21. The method of claim 20 wherein the act of converting is performed in a nitrogen ambient.

22. The method of claim 20 wherein the act of converting is performed in a reducing ambient.

23. The method of claim 20 wherein the act of converting is performed in a nitrogen-supplying reducing ambient.

24. The method of claim 20 wherein the act of converting is performed in an ammonia-containing ambient.

25. The method of claim 20, wherein the act of converting is performed in a hydrogen-containing ambient.

26. The method of claim 20, wherein the art of converting is performed in a helium-containing ambient.

27. The method of claim 20, wherein the art of converting is performed in a neon-containing ambient.

28. The method of claim 20, wherein the art of converting is performed in an argon-containing ambient.

29. The method of claim 20 further comprising exposing the layer having a rough surface to an oxidizing ambient.

30. A method of forming an enhanced-surface-area electrically conductive layer, the method comprising:

providing a layer containing ruthenium oxide;

selecting anneal conditions adapted to convert at least a portion of the ruthenium oxide to ruthenium; and

annealing the layer under said conditions so as to produce a layer having a rough surface.

31. A method of forming a ruthenium-containing enhanced-surface-area electrically conductive layer, the method comprising:

depositing a layer consisting essentially of ruthenium oxide onto a supporting structure; and

annealing the layer in reduced pressure environment in a non-oxidizing ambient so as to substantially convert the ruthenium oxide to ruthenium, leaving a roughened layer consisting essentially of ruthenium on the supporting structure.

32. A method of forming an enhanced-surface-area electrically conductive layer, the method comprising:

forming a layer of conducting material;

forming a layer comprising ruthenium oxide on the layer of conducting material; and

annealing the layer comprising ruthenium oxide so as to convert at least some of the ruthenium oxide to ruthenium so as to produce a layer having a textured surface with a mean feature size of about 100 Angstroms or more.

33. A method of forming an enhanced-surface-area electrically conductive layer, the method comprising:

providing a layer comprising ruthenium oxide;

annealing the layer comprising ruthenium oxide so as to convert at least some of the ruthenium oxide to ruthenium so as to produce a resulting layer having a textured surface with a mean feature size of about 100 Angstroms or more; and

forming a layer of electrically conductive material conformally over the resulting layer such that the surface of the conductive material away from the resulting layer has a textured surface generally corresponding to that of the resulting layer.

34 A method of forming a capacitor, the method comprising:

providing a layer containing ruthenium oxide;

converting least some of the ruthenium oxide to ruthenium so as to produce a resulting layer having a rough surface;

forming a layer of dielectric material over the resulting layer; and

forming a layer of conductive material over the layer of dielectric material.

35. The method of claim 34 wherein the act of forming a layer of dielectric material comprises forming a layer of high-dielectric-constant dielectric material.

36. The method of claim 34, wherein at least some of the ruthenium oxide is converted to ruthenium by annealing the layer at a pressure of 75 torr or less.

37. The method of claim 34, further comprising processing the layer containing ruthenium oxide to define a first electrode.

38. The method of claim 37, wherein the first electrode is defined by an etching process.

39. The method of claim 37, wherein the first electrode is defined by a chemical-mechanical polishing process.

40. The method of claim 37, wherein the first electrode is defined prior to converting at least some of the ruthenium oxide to ruthenium.

41. A method of forming a capacitor, the method comprising:

providing a first layer of electrically conductive material;

forming a layer containing ruthenium oxide on the layer of electrically conductive material;

annealing the layer containing ruthenium oxide so as to convert at least some of the ruthenium oxide to ruthenium and so as to produce a rough resulting surface with a mean grain size of at least about 100 Angstroms;

forming a layer of dielectric material over the layer having a rough surface; and

forming a second layer of conductive material over the layer of dielectric material.

42. The method of claim 41 wherein the act of forming a layer of dielectric material comprises forming a layer of high-dielectric-constant dielectric material.

43. A method of forming a capacitor, the method comprising:

forming a first conductive layer containing tungsten nitride;

forming a layer of dielectric material over the first conductive layer; and

forming a second conductive layer over the layer of dielectric material.

44. The method of claim 43, further comprising annealing at least the first conductive layer at an anneal temperature sufficient to convert a tungsten nitride compound WN into a tungsten nitride compound W_2N.

45. The method of claim 44, wherein the anneal temperature is at least 500 C and the first conductive layer is maintained at the anneal temperature for at least 30 seconds.

46. The method of claim 44, wherein the first conductive layer is formed conformally on a post.

47. The method of claim 44, wherein the first conductive layer is formed conformally in a recess in a substrate.

48. The method of claim 44, where the dielectric layer contains tantalum oxide.

49. A method of increasing a capacitance of a capacitor that includes a tungsten nitride electrode, the method comprising annealing the tungsten nitride layer at an anneal temperature sufficient to convert WN into W_2N.

50. The method of claim 49, wherein the anneal temperature is at least 500 C.

51. An integrated circuit comprising an enhanced-surface-area electrically conductive ruthenium-containing layer having a textured surface with a mean feature size of at least about 100 Angstroms.

52. An integrated circuit comprising an enhanced-surface-area electrically conductive nitrogen-passivated ruthenium-containing layer having a textured surface with a mean feature size of at least about 100 Angstroms.

53. An integrated circuit comprising an enhanced-surface-area electrically conductive nitrogen-passivated and oxygen-passivated ruthenium-containing layer having a textured surface with a mean feature size of at least about 100 Angstroms.

54. An integrated circuit comprising a nitrogen-passivated ruthenium-containing layer.

55. An integrated circuit comprising a nitrogen-passivated and oxygen-passivated ruthenium-containing layer.

56. An integrated circuit comprising an annealed tungsten nitride electrode layer.

57. The integrated circuit of claim 56, wherein the annealed tungsten nitride electrode layer consists essentially of W_2N.

58. The integrated circuit of claim 56, further comprising a dielectric layer of tantalum pentoxide that covers the annealed tungsten nitride layer.

59. A method of forming a passivated layer of ruthenium or ruthenium oxide during fabrication of an electronic device, the method comprising:

providing a layer of ruthenium or ruthenium oxide; and

annealing the layer in a nitrogen-supplying or nitrogen-supplying and reducing ambient so as to passivate the layer.

60. The method of claim 59 further comprising annealing the layer in an oxidizing ambient.

61. The method of claim 59 wherein the act of annealing comprises annealing in an ammonia ambient.

62. The method of claim 59 wherein the act of annealing comprises annealing in a mixture comprising hydrogen and nitrogen.

63. The method of claim 59 wherein the act of annealing comprises annealing in nitrogen.

64. A method of applying a conductive film, the method comprising:

applying a layer of tungsten nitride; and

annealing the tungsten nitride layer.

65. The method of claim 64, wherein the tungsten nitride layer includes a metastable tungsten nitride compound and the tungsten nitride layer is annealed at a temperature sufficient to convert at least some of the metastable compound to a stable compound.

66. A method of forming an array of capacitors, the method comprising:

providing a layer containing ruthenium oxide;

converting at least some of the ruthenium oxide to ruthenium so as to produce a resulting layer having a rough surface;

forming a layer of dielectric material over the resulting layer;

forming a conductive layer on the layer of dielectric material; and

defining an array of electrodes by patterning at least one of the ruthenium oxide layer or the resulting layer.

67. The method of claim 66, wherein the array of electrodes is defined prior to forming the layer of dielectric material.

68. The method of claim 66, wherein the array of electrodes is defined after forming the conductive layer on the dielectric layer.

69. The method of claim 65, wherein the array of electrodes is defined by etching.

70. The method of claim 65, wherein the array of electrodes is defined by chemical-mechanical polishing.

71. A DRAM, comprising an array of capacitors that includes electrodes defined in an enhanced-surface-area electrically conductive layer having a textured surface area with a mean surface area of about 100 Angstroms.

METHODS FOR FORMING AND INTEGRATED CIRCUIT STRUCTURES CONTAINING RUTHENIUM AND TUNGSTEN CONTAINING LAYERS

ABSTRACT

Capacitors having increased capacitance include an enhanced-surface-area (rough-surfaced) electrically conductive layer or other layers that are compatible with the high-dielectric constant materials. In one approach, an enhanced-surface-area electrically conductive layer for such capacitors is formed by processing a ruthenium oxide layer at high temperature at or above 500°C and low pressure 75 torr or below, most desirably 5 torr or below, to produce a roughened ruthenium layer having a textured surface with a mean feature size of at least about 100 Angstroms. The initial ruthenium oxide layer may be provided by chemical vapor deposition techniques or sputtering techniques or the like. The layer may be formed over an underlying electrically conductive layer. The processing may be performed in an inert ambient or in a reducing ambient. A nitrogen-supplying ambient or nitrogen-supplying reducing ambient may be used during the processing or afterwards to passivate the ruthenium for improved compatibility with high-dielectric-constant dielectric materials. Processing in an oxidizing ambient may also be performed to passivate the roughened layer. The roughened layer of ruthenium may be used to form an enhanced-surface-area electrically conductive layer. The resulting enhanced-surface-area electrically conductive layer may form a plate of a storage capacitor in an integrated circuit, such as in a memory cell of a DRAM or the like. In another approach, a tungsten nitride layer is provided as an first electrode of such a capacitor. The capacitor, or at least the tungsten nitride layer, is annealed to increase the capacitance of the capacitor.

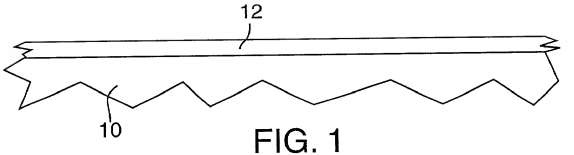


FIG. 1

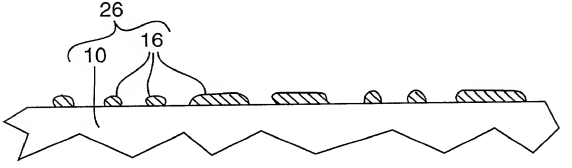


FIG. 2

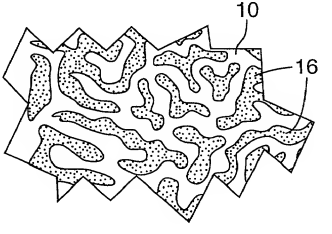


FIG. 3

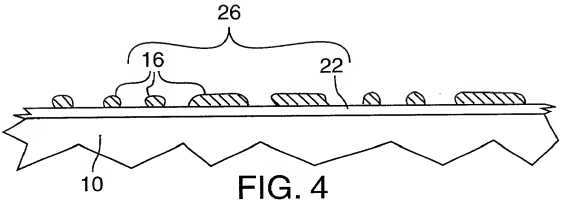


FIG. 4

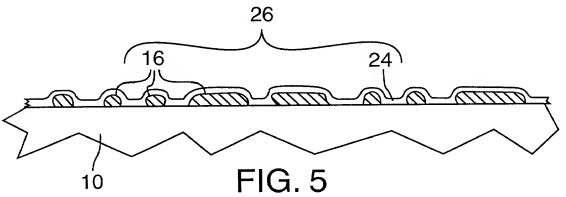


FIG. 5

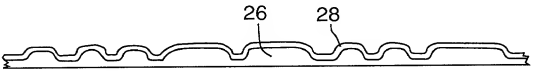


FIG. 6

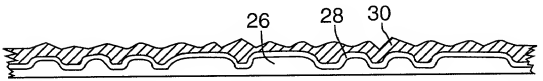


FIG. 7

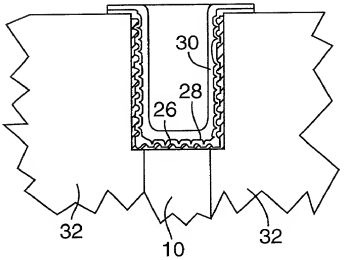


FIG. 8A

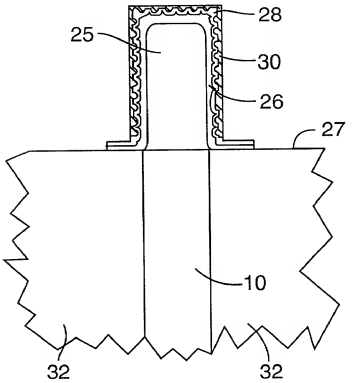


FIG. 8B

FIG. 9A

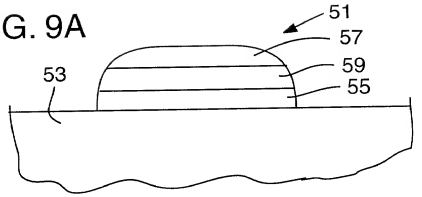


FIG. 9B

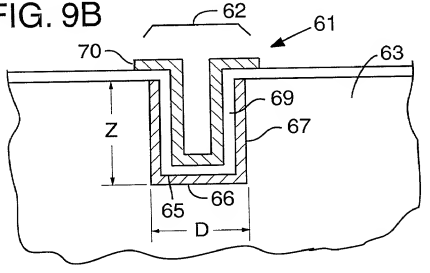
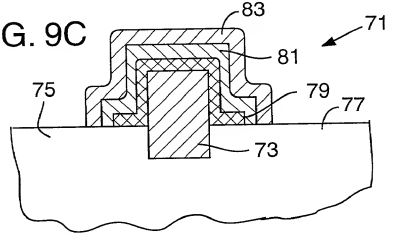


FIG. 9C



DECLARATION OF INVENTOR FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: METHODS FOR FORMING AND INTEGRATED CIRCUIT STRUCTURES CONTAINING RUTHENIUM AND TUNGSTEN CONTAINING LAYERS, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

PRIOR FOREIGN APPLICATIONS:

I hereby state that no applications for foreign patents or inventor's certificates have been filed prior to the date of execution of this declaration.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued therefrom.

* * * * * * * * * * *

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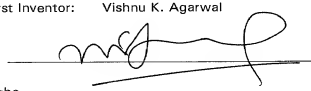
Inventor's Signature  3rd May, 2000

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Art Unit --

Vishnu K. Agarwal, Garo Derderian, Gurtej S. Sandhu, Weimin M. Li, Mark Visokay, Cem Basceri, Sam Yang

Application No.: --

Filed: Herewith

For: METHODS FOR FORMING AND INTEGRATED CIRCUIT STRUCTURES CONTAINING RUTHENIUM AND TUNGSTEN CONTAINING LAYERS

Examiner: --

POWER OF ATTORNEY BY ASSIGNEE AND CERTIFICATE BY ASSIGNEE UNDER 37 CFR § 3.73(b)

TO THE ASSISTANT COMMISSIONER FOR PATENTS
Washington, DC 20231

Sir:

MICRON TECHNOLOGY, INC., the Assignee of the entire right, title and interest in the above-identified patent application by assignment attached hereto, hereby appoints the attorneys and agents of the firm of KLARQUIST SPARKMAN CAMPBELL LEIGH & WHINSTON, LLP, listed as follows:

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GIRARD, Michael P.	38,467	SIEGEL, Susan Alpert	43,121
HARDING, Tanya M.	42,630	SLATER, Stacey C.	36,011
JAKUBEK, Joseph T.	34,190	STEPHENS Jr., Donald L.	34,022
JOHNSON, Michelle L.	36,352	STUART, John W.	24,540
JONES, Michael D.	41,879	VANDENBERG, John D.	31,312
KLARQUIST, Kenneth S.	16,445	WHINSTON, Arthur L.	19,155
KLITZKE II, Ramon A.	30,188	WIGHT, Stephen A.	37,759
LEIGH, James S.	20,434	WINN, Garth A.	33,220
MAURER, Gregory L.	43,781		

and also attorneys Michael L. Lynch (Reg. No. 30,871), Lia M. Pappas (Reg. No. 34,095), W. Eric Webostad (Reg. No. 35,406) and Charles Brantley (Reg.

No. 38,086) of Micron Technology, Inc., as its attorneys with full power of substitution to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

The Assignee certifies that the above-identified Assignment has been reviewed and to the best of Assignee's knowledge and belief, title is in the Assignee, and a copy of the Assignment is submitted herewith.

Please direct all correspondence regarding this application to:

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Date: 5/9/00 By: _____
Name: Michael L. Lynch, Esq.
Title: Chief Patent Counsel

Attachment: Copy of Assignment; Copy of Board of Directors' Resolution